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Dr. Alexander Chenakin is Director of the Frequency Synthesis Group at Phase Matrix, Inc. (San Jose, CA), a leading supplier of high-frequency components, subsystems, and test-and-measurement solutions. He has a proven track record of developing high-performance products for a number of top microwave companies, and is currently overseeing the development of a new generation of fast-switching frequency synthesizers.

An Interview with Alexander Chenakin

Frequency synthesizers are among the most challenging of high-frequency designs. Many approaches have been developed to generate clean output signals, although techniques that achieve low noise often suffer from limited tuning speed. Dr. Chenakin's design team at Phase Matrix is developing solutions to these design trade offs, and *Microwaves & RF* spoke recently with him to hear his thoughts on the current state of microwave frequency synthesis.

MRF: *With so many existing frequency synthesizer architectures, why is there a need for the new approach embodied in your latest products?*

AC: The microwave industry feels persistent pressure to deliver higher-performance, higher-functionality, smaller-size, lower-power consumption, and lower-cost designs. However, the major technology challenge is to achieve fast tuning that is beyond the capabilities of YIG technology historically used in high-performance synthesizers.

MRF: *What are the disadvantages of YIG technology?*

AC: The main disadvantage is low tuning speed due to a high-inductance tuning coil required to generate a strong magnetic field. Besides this, YIG oscillators are traditionally known as expensive, bulky, and power-hungry devices. Although these parameters can be addressed in new YIG designs, the low speed is a fundamental problem inherent in YIG technology.

MRF: *What switching speed requirements are you seeing at present?*

AC: The time spent by the synthesizer jumping between frequencies becomes increasingly valuable since it cannot be used for data processing. A simple example: let's assume you are making a 401 point sweep measurement on an RF IC test using a source with 25 ms switching speed (that is a typical number for a YIG-based synthesizer). In this case, your dead-time per measurement exceeds 10 sec—just for one measurement! If you can use a synthesizer with 100 us switching, your dead-time is reduced to 40 ms. It is quite a significant throughput improvement if you run continuous measurements. Thus, while many systems still work adequately with millisecond switching speeds, newer requirements demand microsecond operation together with comparable spectral purity (such as phase noise and spurious) of the low speed designs. Target numbers are currently in the range of tens of microseconds.

MRF: *What technologies can be used to achieve such speed?*

AC: Direct analog, direct digital, and indirect (or phase locked) approaches are used for modern synthesizers. Each has trade offs. For example, direct-analog synthesizers can provide the best performance in terms of speed, but they are complex and expensive. Direct-digital synthesis (DDS) is fast and reasonably priced, although it still needs to improve in terms of frequency coverage and spurious performance. Thus, the most exciting near-term solutions are likely to be associated with VCO-based PLL synthesizers.

MRF: *What are the advantages of the VCO-based designs?*

AC: Unlike YIGs, VCOs are capable of switching speeds in the microsecond range. With VCOs available as ICs, size, power consumption, and cost are negligible in comparison with YIGs. Besides, VCOs are much less sensitive to microphonic effects due to their extremely low weight and profile.

MRF: *VCOs tune faster than YIGs; however, their phase noise is significantly worse. How do you achieve "YIG-like" noise levels without a YIG?*

AC: The "YIG-like" noise performance varies from definition for a certain offset and output frequency with, let's say, 5 GHz. Although, the numbers differ from vendor to vendor, but typical numbers might be -105 and -125 dBc/Hz, respectively, offset 10 and 100 kHz from a 5-GHz carrier. Current VCOs cannot provide this level of performance, although you can achieve these noise levels by other means, such as by relying on your reference to suppress the VCO noise. Assume your synthesizer includes a 100-MHz oven-stabilized crystal oscillator (OCXO) with -160 dBc/Hz noise floor. Using a standard 20-dB/decade phase-noise degradation rule, you can potentially get -126 dBc/Hz at 5 GHz at both 10 and 100 kHz offsets that corresponds or even exceeds the performance of traditional YIG-based designs.

MRF: *But is it worse at 1 MHz offset?*

AC: It is worse with the same low-cost reference. However, it will be significantly improved with a higher-cost -176 dBc/Hz reference. A better way is to use a combined reference such as an OCXO and CRO (or SAW) oscillator combination. For example, a 3.2 GHz CRO locked to the same OCXO exhibits better than -150 dBc/Hz phase noise at 1 MHz offset.

MRF: *Should the PLL filter bandwidth be wide to utilize the low noise reference benefits at these offsets?*

AC: The loop filter bandwidth must be wide enough, a few MHz or more, to wash out the VCO noise and reach its thermal noise floor. Besides, we are assuming that the reference signal translation is not affected by the synthesizer system (or PLL) noise floor. Nevertheless, the net effect is evident: VCO-based designs can potentially achieve faster tuning speeds and comparable phase noise characteristics of YIGs without the size and power consumption of YIGs.

MRF: *Tell us about your technology for low-noise signal translation.*

AC: We have developed a novel, patent-pending, phase-refining technique to reduce the synthesizer PLL residual noise floor. As you know, the phase noise of a conventional single-loop PLL is proportional to the division ratio of the divider inserted into the loop. In general, by minimizing the ratio, you can improve phase noise. Our technology takes a more radical step by completely removing the divider from the PLL feedback path. Moreover, it inverts the PLL division ratio by applying multiplication within the PLL that improves both phase-noise and spurious characteristics at the same 20 dB/decade rate.

MRF: *What are the drawbacks?*

AC: Removing the divider affects the frequency resolution, so fine resolution must be achieved by other means. We use DDS technology for sub-Hertz steps.

MRF: *Doesn't DDS suffer from high spurious content?*

AC: It does, but there are a number of techniques to reduce these spurs. Signal upconversion followed by division is an example. You can also set your frequency plan in such a manner that your most offensive spurs are outside the PLL bandwidth and, therefore, further suppressed. Our approach does not elevate any spurs in contrast to conventional PLLs.

MRF: *What spurious levels do you achieve?*

AC: Typically -80 dBc or better at 10 GHz. It is hard to measure the spurs at these levels since they become comparable to the spurs generated by the test equipment itself. Thus, we specify this parameter at a -70 dBc level to simplify our testing in production.

MRF: *What is the frequency range?*

AC: The core design covers the 2-to-10-GHz range with a 0.001-Hz step size utilizing a fundamental VCO to achieve the desired output frequency. In contrast to widely used frequency multiplication schemes, this approach eliminates possible spectrum contamination by subharmonic products. Our next model extends the lowest boundary down to 100 MHz providing 0.1-to-10-GHz coverage in the same box; a 20-GHz version is under development.

MRF: *Do you use downconversion for lower frequencies?*

AC: No, we actually use frequency division, which further improves both spurious and phase-noise characteristics. Thus, at the lower end (100 MHz) we achieve better then -150 dBc/Hz at a 10-kHz offset.

MRF: *What is the form factor?*

AC: The 10-GHz unit is 5 x 7 x 1 in.

MRF: *Any special DC requirements?*

AC: Not at all. The synthesizer requires a single +12-VDC bias line only; neither negative nor high-voltage bias is needed. Moreover, the design includes custom active filters to prevent possible signal contamination. One of our customers has successfully biased the synthesizer from a switched DC supply used for laptop computers. All the spurious and noise parameters were in place.

MRF: *How do you synchronize the synthesizer with other equipment?*

AC: The synthesizer includes a highly stable internal OCXO that provides a 10-MHz reference signal to the outside world. The internal oscillator can be automatically locked to an external reference too. We also provide the ability to adjust the internal oscillator frequency (by software means) for temperature and aging compensation.

MRF: *What interfaces are required for a frequency synthesizer?*

AC: Ideally, you want the control interface to be as fast, versatile, and easy to use as possible. The serial peripheral interface (SPI) is the most prevalent, with full duplex communication, relatively high throughput, and flexibility. Another very desirable interface is universal serial bus (USB), which allows instant deployment or just evaluation of the synthesizer from a personal computer.

MRF: *Control interfaces require a central processing unit (CPU) or microcontroller internal to the synthesizer to perform "handshake" or translation functions. Doesn't this requirement slow the switching speed of the synthesizer?*

AC: The CPU does require time to perform the translation functions; therefore, you should be very careful selecting a processor. We use a 32-b, 200-MHz, RISC CPU with enough horse power to keep the processing time to a minimum. Our synthesizers also have internal memory to support a list mode in order to increase the switching speed.

MRF: *How do you apply list mode to increase switching speed?*

AC: Let's assume you have a preset list of frequencies you want to jump between. Knowing these frequencies, you can precalculate and memorize all necessary parameters required to control individual components of the synthesizer. Thus, CPU calculations can be avoided by the time you execute the list mode.

MRF: *Is the internal memory used for any other purpose?*

AC: Certainly. It is used to store various system calibrations such as output power and modulation sensitivity corrections.

MRF: *Does inclusion of the CPU and memory increase the synthesizer size and cost?*

AC: Not really. Very tiny and inexpensive BGA chips are readily available, yet they drastically increase the synthesizer's functionality and productivity.

MRF: *What functionality is desirable in a modern frequency synthesizer?*

AC: Besides getting a clean CW signal, you would most likely want to sweep the synthesizer between certain frequencies with a desired step size and dwell time. Also, it would be nice to control the synthesizer output power, provide power sweep, or completely mute the synthesizer output. Many of our customers frequently require analog power control, various modulation options such as amplitude, frequency, and pulse modulation.

MRF: *Why is the analog control necessary? Isn't the power controlled via a digital interface?*

AC: It is. Moreover, in our design we provide open-loop automatic level control, which is simply a calibration look-up table that corrects output power variations versus frequency and temperature. It is a simple and cost-effective approach for getting flat and repeatable output power readings through all operating conditions. However, in some applications customers want to add a closed-loop automatic level control (ALC), which is accomplished by adding an external coupler and RF detector. The signal from the detector is fed back to the analog power control input to close the loop. This configuration provides precise, instrument-grade output power regardless of the signal match.

MRF: *What output-power level does your synthesizer provide?*

AC: The maximum uncorrected power is close to +20 dBm and can be leveled between –25 and +15 dBm. In addition to the factory preset flat response, the user can set a desirable power-to-frequency slope to compensate for connecting cables as well as other devices external to the synthesizer. The synthesizer's software also includes a programmable equalizer that can easily create virtually any power-to-frequency response.

MRF: *Your synthesizer designs appear to function like benchtop signal generators. Are they intended for that purpose?*

AC: We do not specifically target benchtop applications. Rather, we build a module, or better to say, an engine, which can be put into a benchtop instrument or used in many other applications. However, in terms of performance and technical features, our modules are somewhat comparable to benchtop instruments, while having a much smaller form factor and cost. By the way, you can instantly build your own signal generator by simply plugging a USB cable into your laptop and turning on the bias. We provide software that emulates basic signal generator functions, so you can control all the bells and whistles from your computer screen.

MRF: *Your synthesizers might be low-cost options for some test setups?*

AC: That is true. If you need to test the third-order-intercept characteristics of your mixer, you generally have to connect three benchtop signal generators. Using synthesizer modules such as this can result in significant savings in cost and benchtop space.

MRF: *What markets do you plan to target these modules?*

AC: There is a certain market segment not presently addressed by current microwave synthesizer vendors. There are a number of synthesizer modules (or bricks), which are small and inexpensive; however, they don't quite have the necessary technical characteristics and features. On the other hand, sophisticated benchtop and rack-mountable units are bulky and expensive. Our new synthesizer technology—with its superior performance, compact size, and low cost—bridges this gap addressing both traditional test-and-measurement equipment as well as emerging synthetic instrumentation. In addition to the test-and-measurement community, it will be also beneficial in applications within many other markets from telecommunications to signal-gathering systems.

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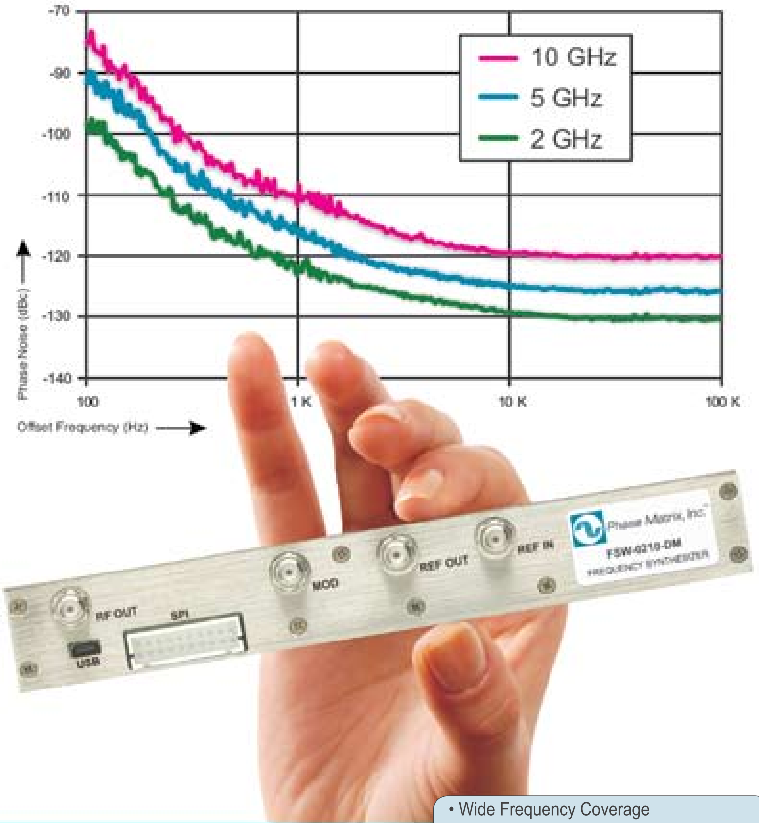

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